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(54) **Method of surface treatment of semiconductor substrates**

(57) This invention relates to methods for treatment of semiconductor substrates and in particular a method of etching a trench in a semiconductor substrate in a reactor chamber using alternatively reactive ion etching and depositing a passivation layer by chemical vapour deposition, wherein one or more of the following parameters: gas flow rates, chamber pressure, plasma power, substrate bias, etch rate, deposition rate, cycle time and etching/deposition ratio vary with time.

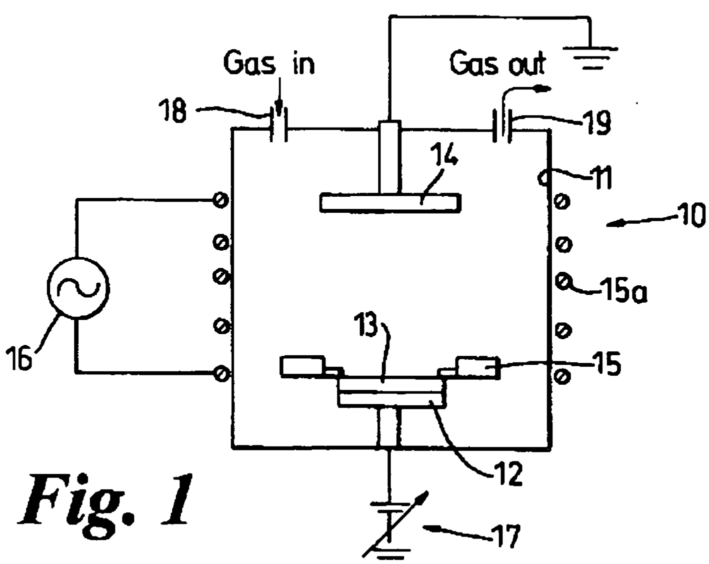

Fig. 1

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Description

This invention relates to methods for treatment for semiconductor substrates and in particular, but not exclusively, to methods of depositing a sidewall passivation layer on etched features and methods of etching such features including the passivation method.

It is known to anisotropically etch trenches or recesses in silicon using methods which combine etching and deposition. The intention is to generate an anisotropic etch, whilst protecting the sidewalls of the trench or recess formed by laying down a passivation layer.

Such methods are for example shown in US-A-4579623, EP-A-2497023, EP-A-0200951, WO-A-94114187 and US-A-4985114. These all describe either using a mixture of deposition and etching gases or alternate etching and deposition steps. The general perception is that mixing the gases is less effective because the two processes tend to be self cancelling and indeed the prejudice is towards completely alternate steps.

Other approaches are described in EP-A-0383570, US-A-4943344 and US-A-4992136. All of these seek to maintain the substrate at a low temperature and at first, somewhat unusually, uses burst of high energy ions during etching to remove unwanted deposits from the sidewalls.

The continuous trend in semiconductor manufacture is for features of ever increasing aspect ratio, whence the sidewall profile and the surface roughness on the sidewalls, becomes more significant the smaller the width of the feature. Current proposals tend to produce a rather bowed or reentrant sidewall profile as well as rough sidewalls and/or bases to the formations depending on the process being run.

The manifestation of the various problems depends on the application and the respective processing requirements, silicon exposed area (unmasked substrate areas), etch depth, aspect ratio, side wall profile and substrate topography.

The method of this invention, in at least some embodiments, addresses or reduces these various problems.

From one aspect the invention consists in a method of etching a trench in a semiconductor substrate in a reactor chamber using alternately reactive ion etching and depositing a passivation layer by chemical vapour deposition, wherein one or more of the following parameters: gas flow rates, chamber pressure, plasma power, substrate bias etc rate, deposition rate, cycle time and etching/deposition ratio vary with time. The variation may be periodic.

The etching and deposition steps may overlap and etching and deposition gases may be mixed.

The method may include pumping out the chamber between the etching and deposition and/or between deposition and etching, in which case the pump may continue until

$$\frac{Ppa}{Ppa + Ppb} < x$$

wherein Ppa is the partial pressure of the gas (A) used in the preceding step,
Ppb is the partial pressure of the gas (B) to be used in the subsequent step,
and
x is the percentage at which the process rate of the process associated with gas (A) drops off from an essentially steady state.

The etching and deposition gas flows may be continuously or abruptly variable. For example the deposition and etching gases may be supplied so that their flow rates are sinusoidal and out of phase. The amplitude of any of these parameters may be variable within cycles and as between cycles.

It is particularly preferred that the deposition rate is enhanced and/or etch is reduced during at least the first cycle and in appropriate circumstances in the first few cycles for example in the second to fourth cycles.

The etch rate may be reduced by one or more of the following

(a) the introduction of a scavenging gas
(b) a reduction in plasma power
(c) a reduction in cycle time and
(d) a reduction in gas flow
(e) varying the chamber pressure

The deposition rate may be enhanced by one or more of the following

(a) an increase in plasma power
(b) an increase in cycle time
(c) an increase in gas flow rate
(d) an increase in deposition species density

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(b) a reduction in plasma power
(c) a reduction in cycle time and
(d) a reduction in gas flow
(e) varying the chamber pressure

The deposition rate may be enhanced by one or more of the following

(a) an increase in plasma power
(b) an increase in cycle time
(c) an increase in gas flow rate
(d) an increase in deposition species density

(e) varying the chamber pressure

Other advantageous features of the method are that the etch and/or deposition steps may have periods of less than 7.5 seconds or even 5 seconds to reduce surface roughness; the etch gas may be CF_x or XeF_2 and may include one or more high atomic mass halides to reduce spontaneous etch; and the chamber pressure may be reduced and/or the flow rate increased during deposition particularly for shallow high aspect ratio etching where it may be accompanied by increased self bias (e.g. voltage >20eV or indeed >100eV).

The deposition step may use a hydrocarbon deposition gas to deposit a carbon or hydrocarbon layer. The gas may include O, N or F elements and the deposited layer may be Nitrogen or Flourine doped.

The substrate may rest freely on a support in the chamber when back cooling would be an issue. Alternatively the substrate may be clamped and its temperature may be controlled, to lie, for example, in the range -100°c to 100°c. The temperature of the chamber can also advantageously be controlled to the same temperature range as the wafer to reduce condensation on to the chamber or its furniture to reduce base roughness.

The substrate may be GaAs, GaP, GaN, GaSo, SiGe, Mo, W or Ta and in this case the etch gas may particularly preferably be one or a combination of Cl_2, BCl_3 $SiCl_4$, $SiCl_2H_2$ CH_xCl_y, C_xCl_y, or CH_x with or without H or an inert gas. Cl_2 is particularly preferred. The deposition gas may be one or a combination of CH_x, CH_xCl_y, or C_xCl_y, with or without H, or an inert gas CH_4 or CH_2Cl_2 are particularly preferred.

Although the invention has been defined above it is to be understood that it includes any inventive combination of the features set out above or in the following description.

The invention may be performed in various ways and a specific embodiment will now be described by way of example, with reference to the accompanying drawings in which:

Figure 1 is a schematic view of a reactor for processing semiconductors;
Figure 2 is a schematic illustration of a trench formed by a prior art method;
Figure 3 is an enlarged view of the mouth of the trench shown in Figure 2;
Figure 4 is a plot of etch rate of silicon against the percentage of CH_4 in H_2;
Figure 5 is a plot of step coverage against the percentage of CH_4 in H_2 for different mean ion energies;
Figure 6 is a diagram illustrating various possible synchronisations between gases and operating parameters of the Figure 1 apparatus;
Figure 7 is a diagram corresponding to Figure 6, but illustrating an alternative operating scenario;
Figure 8 is a plot of the etch rate of silicon against a partial pressure ratio;
Figure 9(i) is a schematic representation of parameter ramping for deep anisotropic profile control whilst 9(ii) illustrates ramping more generally;
Figures 10 and 11 are SEM's of a trench formed in accordance with the prior art, Figure 11 being an enlargement of the mouth of Figure 10;
Figures 12 and 13 are corresponding SEM's for a trench formed by the Applicants' process in which an abrupt transition in process parameters has occurred;
Figure 14 corresponds to Figure 12 except ramped parameters have been utilised;
Figure 15 is a plot of deposition rate against RF Platen Power at a variety of chamber pressures;
Figure 16 is a SEM of a prior art high aspect ratio trench;
Figure 17 is a corresponding SEM using the Applicants' process with abrupt transitions;
Figure 18 is a SEM of a high aspect ratio trench formed by the Applicants' process whilst using ramped transitions.
Figures 19(a) and 19(b) are tables setting out the process conditions used for the trenches shown in Figures 14 and 18 respectively;
Figure 20 is a diagram showing the synchronisation of Deposition and Etch gas during the initial cycles of the Applicants' process; and
Figure 21 is a diagram showing an alternative approach to Figure 20 utilising a scavenger gas.

Figure 1 illustrates schematically a prior art reactor chamber 10, which is suitable for use both in reactive ion etching and chemical vapour deposition. Typically a vacuum chamber 11 incorporates a support electrode 12 for receiving a semiconductor wafer 13 and a further spaced electrode 14. The wafer 13 is pressed against the support 12 by a clamp 15 and is usually cooled, by backside cooling means (not shown).

The chamber 11 is surrounded by a coil 15a and fed by a RF source 16 which is used to induce a plasma in the chamber 11 between the electrodes 12 and 14. Alternatively a microwave power supply may be used to create the plasma. In both cases there is a need to create a plasma bias, which can be either RF or DC and can be connected to the support electrode 12 so as to influence the passage of ions from the plasma down on to the wafer 13. An example of such an adjustable bias means is indicated at 17. The chamber is provided with a gas inlet port 18 through which deposition or etched gases can be introduced and an exhaust port 19 for the removal of gaseous process products

and any excess process gas. The operation of such a reactor in either the RIE or CVD modes is well understood in the art.

When etching trenches, etches, vias or other formations on the surface of a semiconductor wafer or substrates, the usual practice is to deposit a photo-resist mask with openings revealing portions of the substrate. Etched gases are introduced into the chamber and a number of steps are then taken to attempt to ensure that the etching process is anisotropic in a downward direction so that there is as little etching of the sidewalls of the formation as possible. For a variety of reasons it is difficult in practice to achieve true anisotropic etching and various attempts are made to deposit passivating materials onto the sidewalls so that the material can be sacrificially etched. The most successful to date of such systems is probably that described in WO-A-94114187 and this system is schematically illustrated in Figure 2. The process described in that document uses sequential and discrete etch and deposition steps so that after the first etched step the sidewalls are undercut as shown at 20 and this undercut is then protected by a deposited passivation layer 21. As can be seen from Figure 2 this arrangement produces a rough sidewall and as the etched steps increase, or indeed the aspect ratio increases, there can be bowing or re-entrant notching in the profile. The prior art documents describe the deposition of CF_x passivation layers.

The Applicant proposes a series of improvements to such processes to enable the formation of more smooth walled formations and particularly better quality deep and/or high aspect ratio formations. For convenience the description will therefore be divided into sections.

1. <u>Passivation</u>

As has been mentioned above previous proposals deposit a passivation layer of the form CF_x. The Applicants propose passivating the sidewalls with carbon or hydrocarbon layers which will provide significantly higher bond energies, particularly if deposited under high self- bias so that the graphitic phase is at least partially removed.

If these films or layers are also desirably deposited at high self biases eg. 20eV upwards and preferably over 100 eV, there is an additional significant advantage when it comes to high aspect ratio formations, because the high self-bias ensures that the transport of the depositing material down to the base of the formation being etched is enhanced to prevent re-entrant sidewall etching. This transportation effect can also be improved by progressively reducing the chamber pressure and/or increasing the gas flow rate, so as to reduce the residence time. In some arrangements it may be desirable to drive the deposition to such an extent that a positively tapered, or v-shaped formation is achieved. In the particular case of shallow (<20μm) high aspect ratio trenches, the feature opening size (or critical dimension) can be in the <0.5μm range.

The hydrocarbon (H-C) films formed by this passivation have significant advantages over the prior art fluorocarbon films.

The H-C films can for example be readily removed after etching processing has been completed by dry ashing (oxygen plasma) treatment. This can be particularly important in he formation of MEMS (micro-electro-mechanical systems) where wet processing can result in sticking of resonant structures which are separated by high aspect trenches. In other applications, eg. optical or biomedical devices, it can be essential to remove completely the side wall layer.

The H-C films may be deposited from a wide range of H-C precursors (eg. CH_4, C_2H_4, C_3H_6, C_4H_8, C_2H_2. etc. including high molecular weight aromatic H-C's). These may be mixed with noble gases and/or H_2. An oxygen source gas can also be added (eg CO, CO_2, O_2 etc.) can be used to control the phase balance of the film during deposition. The oxygen will tend to remove the graphitic phase (sp^2) of the carbon leaving the harder (sp^3) phase. Thus, the proportion of oxygen present will affect the characteristics o the film or layer, which is finally deposited.

As has been mentioned above H_2 can be mixed in with the H-C precursor. H_2 will preferentially etch silicon and if the proportions are correctly selected, it is possible to achieve side wall passivation, whilst continuing the etching of the base of the hole during passivation phase.

The preferred procedure for this is to mix the selected H-C precursor (eg. CH_4) with H_2 and process a mask patterned silicon surface with the mixture in the apparatus, which is to be used for the proposed etch procedure. The silicon etch rate is plotted as a function of CH_4 concentration in H_2 and an example of such a plot is shown in Figure 4. It will be noted that the etch rate increases from an initial steady state with increasing percentage of CH_4 to a peak before decreasing to zero.

It is believed the graph illustrates the following mechanisms taking place. In the initial steady state portion the etch is essentially dominated by the action of H_2 to form SiHx reaction products. At around 10% of CH_4 in H_2, the CH_4 etching of the substrate becomes significant (by forming Si(CHx)y products) and the etch rate increases. Deposition of a hydrocarbon layer is taking place throughout although due to the etching there is no net deposition on this part of the graph. Eventually, the deposition begins to dominate the etching process until at around 38% for CH_4, net deposition occurs.

It has been determined that these varying characteristics can be utilised in two different ways. If high self bias or there is high mean ion energy, eg. >100ev, the layer or coating laid down is relatively hard because the reduced graphitic

phase and the process can be operated in the rising portion of the etch rate graph, because the coating is much more resistant to etching, than the silicon substrate. It is thus possible to etch the silicon throughout the deposition phase. Selectivies exceeding 100:1 to mask or resist are readily achieved. It should particularly be noted that, whilst there is a significant removal of the graphitic phase due to ion bombardment of the mask 22, the high directionality of the ions means that the side wall coating is relatively untouched.

The process can also be operated at low mean ion energies either with a H-C precursor alone or with H_2 dilution. In that latter case it is preferred that the process is operated in the descending part of the etch graph. ie. for CH_4 at a percentage >18% but <38% when net deposition occurs. Typically the range for CH_4 would be 18% to 30%.

The low values of mean ion energy during the polymer deposition are believed to be beneficial in allowing high mask selectivies. Under these lower rf bias conditions, the selectivity increase to infinity over a wide passivation deposition window. So if high selectivity is required, the low mean ion energy approach offers advantages. Figure 5 illustrates the step coverage (side wall deposition measured at 50% of the step height versus surface deposition) for H-C films using CH_4 and H_2 under a range of conditions including the two embodiments described above. Figure 5 shows that high ion energies increase the step coverage, but even with low bias conditions, there is sufficient passivation to protect against lateral etching. Further, in this latter case the higher deposition rate serves further to enhance the mask selectivity. The deposition rate at low ion energies is a factor of two greater over the 100ev case.

It will thus be appreciated that by using these techniques the user can essentially select the combination of etch rate and selectivity, which most suits his proposed structure. Further the enhancement of mask selectivity can be used to either increase the etch rate and/or reduce the notching.

Figure 6 illustrates how various parameters of the process may be synchronised. 6d shows continuous and unchanging coil power, whilst at 6e the coil power is switched to enhance the etch or deposition step and the power during etch may be different to that selected for deposition depending on the process performance required. 6e, by way of example, illustrates a higher coil power during deposition.

6f to i show similar variations in bias power. 6f has a high bias power during etch to allow ease of removal of he passivation film, whilst 6g illustrates the use of an initial higher power pulse to enhance this removal process, whilst maintaining the mean ion energy lower, with resultant selectivity benefits. 6h is a combination of 6f and 6g for when the higher ion energies are required during etching (eg. with deep trenches). 6i simply shows that bias may be off during deposition.

In some processes, at least, the acceptable segregation period of the gases is determined by the residual partial pressure of gas A (Ppa) which can be tolerated in the partial pressure of gas B(Ppb). This minimum value of Ppa in Ppb is established from the characteristic process rate (etch or deposition) as a function of Ppa/(Ppa + Ppb).

In Figure 8, Gas A is 20% $CH_4 + H_2$, whilst gas B is SF_6. It will seen that where Ppa/(Ppa + Ppb) < 5%, the process rate is substantially steady state. For typical practical conditions a pump out time of less than 1.5 seconds will suffice and a plasma can be maintained for over 65% of the total cycle time where the process steps are of the order of 2 to 3 secs and over 80% when the steps are over 5 seconds long. A suitable synchronisation arrangement is shown in Figure 7. It will be noted that the etch precedes the pump out as it is desirable to prevent a mixing of the deposition and etch step gasses. Prior art proposals (eg. U.S.A. 4985114) propose switching off or reducing deposition gas flow for a long period before the plasma is switched on. This can mean that the plasma power is on only for a small portion of the total cycle times leading to a significant reduction in etch rate. The Applicants propose that the chamber should be pumped out between at least some of the gas changeovers, but care must be taken to maintain pressure and gas flow stabilisation. Preferably high response speed mass flow controllers (rise times (100ms) and automatic pressure controllers (angle change and stabilise in (300 ms) are used.

The Applicants have established (see Figure 8) that the pump out time period necessary to avoid the etch being compromised by the deposition gases. However pump out could precede the etch step or both etch and deposition step depending on the precise process being run. Pump out also reduces micro-loading (which is described in USA 4985114) and is beneficial high aspect ratio etching as described below.

Many of the parameters, which are varied can be 'ramped' as general illustrated in Figure 9(II). This means that they progressively increase or decrease cycle by cycle in amplitude or period, rather than changing abruptly between cycles. In the case of the pump out, ramping can be used to allow mixing at the start of the process allowing sidewall notching to be reduced or eliminated as discussed below.

Typical process parameters are as follows:

1. Deposition step	
CH_4 step time	2-15 seconds ; 4-6 seconds preferred
H_2 step time	2-15 seconds ; 4-6 seconds preferred
Coil rf power	600W-1 kW ; 800W preferred

(continued)

1. Deposition step	
Bias rf power	High mean in energy case: 500W-300W-100W preferred Low mean in energy case: 0W-30W-10W preferred
Pressure	2 mTorr-50 mTorr; 20 mTorr preferred

2. Etch Step	
SF_6 step time	2-15 seconds ; 4-6 seconds preferred
Coil rf power	600W-1kW -800W preferred
Bias rf power	High mean ion energy case: 500W-300W; 150W preferred Low mean ion energy case: 0W-30W; 15W preferred
Pressure	2 mTorr-50 mTorr; 30 mTorr preferred.

2. Etch/Deposition Relationship

The Applicant has determined that the prior art approaches are essentially too simplistic, because they neither allow for changing conditions during a particular process nor for the different requirements or different types of formation. Further the prior art does not address the difficulties of deep etching.

Thus contrary to the teaching of WO-A-94114187 the Applicant believes that it will often be beneficial to overlap the etch and passivation or deposition steps so that the surface wall roughness indicated in Figure 2 can be significantly reduced. The Applicant has also established that surprisingly the rigid sequential square wave stepping which has previously been used is far from ideal. In many instances, it will be desirable to use smooth transitions between the stages, particularly where overlap occurs, when reduction of the etch rate is acceptable. Thus one preferred arrangement is for the gas flow rates of the etch and deposition gases to vary with time in a sinusoidal manner the two "wave forms" being out of phase, preferably by close to 90°. As the sidewall roughness is essentially a manifestation of the enhanced lateral etch component, it can be reduced by limiting this component of the etch. The desired effect can be obtained in one of a number of ways: partially mixing the passivation and etch steps (overlapping) ; minimising the etch (and hence corresponding passivation) duration; reducing the etch product volatility by reducing the water temperature; adding passivation component to the etch gas e.g. SF_6 with added 0, N, C, CF_x, CH_x, or replacing the etch gas with one of lower reactive species liberating gas such as SF_6 replaced by CF_x etc.

The Applicant has also appreciated that changes in the levels of etching and deposition are desirable at different stages within the process. The Applicants propose that the first cycle or the first few cycles should have an enhanced deposition by increasing the period of deposition, the deposition rate, or any other suitable means. Equally or alternatively the etch rate or time can be reduced.

As has briefly been indicated before, it also can become progressively more difficult to deposit material as the formation or trench gets deeper and/or the aspect ratio increases. By controlling the amplitude o one or more of the gas flow rates, chamber pressure, plasma power, biasing power, cycle time, substrate etching/deposition ratio, the system can be tuned in an appropriate manner to achieve good anisotropic etching with proper sidewall passivation.

These and related techniques can be utilised to overcome a number of problems in the etch profile:

a. Sidewall Notching

The sidewall notching' problem is particularly sensitive to the exposed silicon area (worse at low exposed areas <30%) and is also correspondingly worse at high silicon mean etch rates. The Applicants believe such notching to be caused by a relatively high concentration of etch species, during the initial etch/deposition cycles. Therefore the solutions adopted by the Applicants are to either enhance the passivation or quench etch species during the first cycles. The latter can be achieved either by process adjustment (ramping one of more of the parameters) or by placing a material within the reactor which will consume (by chemical reaction) the etch species, such as Si, Ti, W etc. reacting with the F etchant. Such chemical loading has the drawback of reducing the mean etch rate, as the quenching is only necessary for the first few etch steps. Thus, process adjustment solutions are considered superior.

It is desirable to reduce/eliminate the sidewall notching without compromising or degrading any of the other aspects of the etch, such as etch rate, profile control, selectivity etc. Investigations by the Applicants have shown the approach of 'reducing the etch species concentration at the start of etch' is best controlled by beginning with process with:

a. fluorine scavenging gas introduction or
b. low coil power or
c. low etch cycle time (step duration) or
d. low etch gas flow or
e. an increase of the corresponding parameters a to d above during the passivation cycle
f. a combination of the above.

followed by increasing the respective parameter(s) to normal pre-optimised etch conditions such as are illustrated in Figure 6. The increase can either be abrupt (that is using say a step change in the a to f parameters) or ramped. The results of these two approaches are now presented, in comparison to the teachings of the prior art.

The nature of the problem (resulting from directly applying the prior art) during a silicon trench etch is shown in Figure 3 schematically and in the SEM's (scanning electron micrographs) shown in Figure 10 and 11. These Figures show that for a 1.7μm initial trench opening the CD loss is 1.2μm (70%), whilst the notch width is up to 0.37μm. Such values of CD loss are unacceptable for the majority of applications.

However by using the Applicants method (eg. a.to f.), of varying the process parameters during the initial cyclic etch process, the notched sidewall can be modified. If abrupt steps are used to vary the process parameters, abrupt transitions are produced in the sidewall profiles. The SEMs in Figures 12 and 13 illustrate this for different process parameters. In Figure 12, the transition in the process parameters is clearly marked as an abrupt transition in the sidewall profile at the point of parameter change (after 8.5μm etch depth). (Note that the sidewall notches have been eliminated.) Figure 13 illustrates yet another process parameter abrupt/step change. Here the sidewall passivation is high enough to result in a positive profile (and no notching) for the first 2μm. When the reduced passivation conditions are applied, it is characterised by the transition in sidewall angle and reappearance of the notching.

By using the 'ramped' parameter approach, the notching can be eliminated, as well as producing a smooth sidewall profile without any abrupt transition, see the SEM in Figure 14. This shows a 22μm deep trench etch, with a smooth positive profile and no CD loss, whilst maintaining etch rate comparable to the non-ramped high underact process. The process conditions used in this case are given in Figure 19a.

<u>b. Profile control during deep high aspect ratio etching</u>

The teachings of the prior art are limited where high aspect ratio (>10:1) etching is required. Whilst the limitations and solutions are discussed here for relatively deep etching (>200μm), there is equal relevance for shallow high aspect ratio etching, even for very low values of CD, such as <0.5μm.

One of the basic mechanisms, that distinguishes high aspect ratio etching, is the diffusion of the etching (and passivation) reactive precursors as well as etch products. This species transport phenomenon was investigated for the passivation step. The results show clearly that the transport of sidewall passivation species to the base of deep trenches is improved at low pressure. Increasing platen power also improves this, see Figure 15. The graph illustrates the improved passivation towards the base of the trench as the pressure decreases and the rf bias power increases. This data was obtained by firstly etching 200μm deep trenches, then using the passivation step only and measuring the variation of sidewall passivation with depth using an SEM. This supports the variation of passivation with etch depth, and further supports the suggestion that the optimum process conditions vary with etch depth.

The limitations of applying the prior art for such a high aspect ratio process is shown by the SEM in figure 16. It should be noted that this relatively high passivation to etch ratio fixed parameter process still does result in initial sidewall notching, but the SEM magnification is not sufficiently high to show this for the 10μm CD, 230μm deep trench etch. From the trends shown in Figure 15, the profile can be somewhat improved by operating at under the desired high bias rf power and low pressure conditions. However as a fixed parameter process, the high bias and low pressure conditions significantly degrades the mask selectivity (from >100:1 to <20:1) as the ion energy is increased. Using an abrupt parameter variation results in a corresponding abrupt sidewall change, as shown by the SEM in Figure 17. Ramping the following parameters: increasing platen power, decreasing pressure, increasing cycle times and gas flows; does produce the desired results whilst maintaining reasonably high selectivities >75:1, see Figure 18. Here the SEM shows a 295μm deep, 12μm CD trench etch (25:1 aspect ratio). The process conditions used in this case are given in Figure 19b.

Figure 20 illustrates a synchronisation between deposition and etch gases which have been used for the initial cycles to reduce side wall notching. Typical operating conditions are given in Figure 19a and its associated SEM in Figure 14. Figure 21 illustrates a synchronisation reference to using a scavenger gas with method (a) of side wall notch reduction technique. The dotted line indicates the alternative of the scavenger gas flow rate being decreasingly ramped.

Figure 9i shows a synchronisation for achieving a deep high aspect ratio anisotropic etch although the ramping technique shown can also be used for side wall notch reduction. The conditions of Figure 19b can be used to achieve the results shown in Figure 18.

Returning to Figure 9i:

1. Shows an average pressure ramp. Note the pressure changes from low to high as the cycle changes from deposition to etch respectively. The ramp down of pressure then results in the pressure decreasing for both etch and passivation cycles.
2. This shows a rf bias power ramp. Note the bias change from low to high as the cycle changes from deposition to etch respectively. This is in synchronisation with the pressure change discussed above. The ramp up of bias refers to the deposition step only in this case.
3. This shows another example of a rf bias power ramp. Again the bias changes from low to high as the cycle changes from deposition to etch respectively, in synchronisation to the pressure. The ramp up of bias refers to both the deposition step and etch step in this case.

In Figure 9ii general parameter ramping is illustrated. These examples serve to illustrate cycle time and step time ramping respectively.

4. This shows a cycle time ramp, where the magnitude of the parameter (such as gas flow rates, pressure, rf powers, etc) is not ramped. In some applications this would serve as an alternative to the 'magnitude' ramping in the above cases.
5. This shows a cycle time ramp, where the magnitude of the parameter (such as gas flow rates, pressure, rf powers, etc.) is ramped in addition. Note, the parameter ramp may be increasing or decreasing in magnitude, and the decrease may be to either zero or a non-zero value.

3. Etch Gases

Whilst any suitable etch gases may be used, the Applicant has found that certain gases or mixture can be beneficial.

Thus, it has been suggested in WO-A-94114187 that it is undesirable to have any passivating gas in the etch stage, because it affects the process rate. However, the Applicant has determined, that this procedure can significantly improve the quality of the sidewall trenches formed and it is proposed that the etched gas may have added to it such passivating gases as O,N,C, hydrocarbons, hydro-halo carbons and/or halo-carbons. Equally, and for the same purpose, it is desirable to reduce the chemical reactivity of the etched gas and the Applicant proposes using CF_x for example with higher atomic mass halides such as Cl, Br or I. However XeF_2 and other etch gases may be used.

The degree of sidewall roughness can also alternatively be reduced by limiting the cycle times. For example it has been discovered that it is desirable to limit the etch and deposition periods to less than 7.5 seconds and preferably less than 5 seconds.

4. Gallium Arsenide and other materials

Previous proposals have all related to trench formation in silicon. The Applicant has appreciated that by using suitable passivation, anisotropic etching of Gallium Arsenide and indeed, other etchable material, can be achieved. For example it is proposed that Gallium Arsenide be etched with Cl_2 with or without passivating or etch enhancing gases, but in general it has been determined that this technique is much more successful with the carbon or hydro carbon passivation proposed above. If traditional CF_x chemistry is used etch inhibiting compounds can be created which increase surface roughness or limit the etch. For Gallium Arsenide lower temperatures may be desirable as may be the use of a low pressure, high plasma density reactor. Suitable etch chemistries have already been listed in the preamble to this specification.

Claims

1. A method of etching a feature in a semiconductor substrate in a reactor chamber using alternately reactive ion etching and depositing a passivation layer by chemical vapour deposition, wherein one or more of the following parameters: gas flow rates, chamber pressure, plasma power, substrate bias, etch rate, deposition rate, cycle time, and etching/deposition ratio vary with time.

2. A method as claimed in claim 1 wherein the variation is periodic.

3. A method as claimed in claim 2, wherein the parameter or parameters vary as a sinusoidal, square, or saw tooth waveform or a combination of these.

4. A method as claimed in any one of the preceding claims wherein the variations in the parameter or parameters

are ramped.

5. A method of etching as claimed in any one of the preceding claims wherein the etching and deposition steps overlap.

6. A method as claimed in any one of the preceding claims wherein the etching and deposition gases are mixed.

7. A method as claimed in any one of the preceding claims including pumping out the chamber between etching and deposition and/or between deposition and etching.

8. A method as claimed in claim 7 wherein the pump out continues until

$$\frac{Ppa}{Ppa + Ppb} < x$$

wherien Ppa is the partial pressure of the gas (A) used in the preceding step,
Ppb is the partial pressure of the gas (B) to be used in the subsequent step,
and
x is one percentage at which the process rate of the process associated with gas (A) drops off from an essentially steady state.

9. A method as claimed in any of the preceding claims, wherein the amplitude of the parameters is variable within a cycle or as bazween cycles.

10. A method as claimed in any one of the preceding claims wherein the etch rate is reduced and/or the deposition rate is enhanced during the first cycle or for up to at least the first few cycles.

11. A method as claimed in claim 10 wherein the etch rate is reduced by one or more of the following:

(a) the introduction of a scavenging gas
(b) a reduction in plasma power
(c) a reduction in cycle time and
(d) a reduction in gas flow
(e) varying the chamber pressure

12. A method as claimed in claim 10 or claim 11 wherein the deposition rate is enhanced by one or more of the following:

(a) an increase in plasma power
(b) an increase in cycle time
(c) an increase in gas flow rate
(d) an increase in deposition species density
(e) varying the chamber pressure

13. A method as claimed in any one of claims 1 to 12 wherein the chamber pressure is reduced as a function of feature depth.

14. A method as claimed in any one of claims 1 to 12 wherein the substrate bias is increased as a function of feature depth.

15. A method as claimed in any one of the preceding claims, including depositing a mask having openings prior to etching.

16. A method as claimed in any one of claims 10 to 15, wherein the mask is enhanced by or is itself deposited as a carbon or hydrocarbon layer.

17. A method as claimed in any one of the preceding claims, wherein the etch and/or depositions have periods of less than 7.5 secs or 5 secs.

18. A method as claimed in any one of the preceding claims, wherein the etch gas is CF_x or XeF_2.

19. A method as claimed in any one of the preceding claims, wherein the etch gas includes one or more higher atomic mass halides.

20. A method as claimed in any one of the preceding claims, wherein the chamber pressure is reduced and/or the flow rate is increased during deposition.

21. A method as claimed in any one of the preceding claims, wherein the substrate rest freely on a support in the chamber to be heated to equilibrium by the plasma.

22. A method as claimed in any one of claims 1 to 21, wherein the substrate is maintained at between -100°C and 100°C.

23. A method as claimed in any one of the preceding claims, wherein the substrate is GaAs, GaP, GaN, GaSb, SiGe, Ge, Mo, W or Ta.

24. A method as claimed in claim 23, wherein the etch gas is one or a combination of $C1_2$, BCl_3, $SiCl_4$, $SiCl_2H_2$, CH_xC1_y, C_xC1_y, CH_x with or without H or an inert gas.

25. A method as claimed in claim 23 or claim 24, wherein the deposition gas is one or a combination of CH_xH_y, CH_x, CH_xC1_y or C_xC1_y with or without H, or an inert gas.

26. A method as claimed in any one of the preceding claims, wherein the deposition gas is a hydrocarbon gas to deposit a carbon or hydrocarbon layer.

27. A method as claimed in claim 26, wherein the deposition gas includes O, N or F elements and/or is mixed with H_2.

28. A method as claimed in claim 27, wherein the deposited layer is Nitrogen and/or Fluorine dopes.

29. A method of etching a feature in a semiconductor substrate including alternately etching and depositing a passivation later wherein one deposition rate is enhanced and/or etch rate is reduced during at least the first cycle.

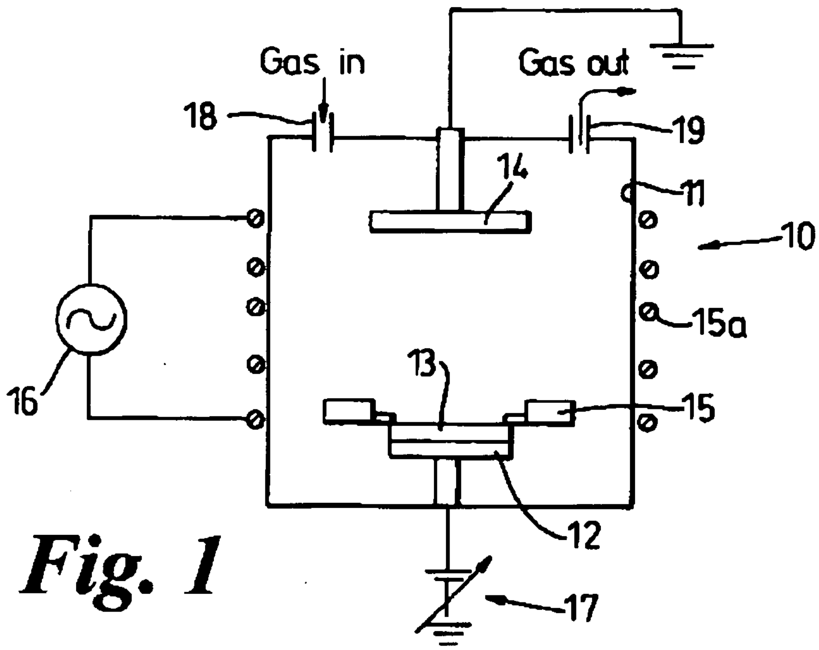


Fig. 1

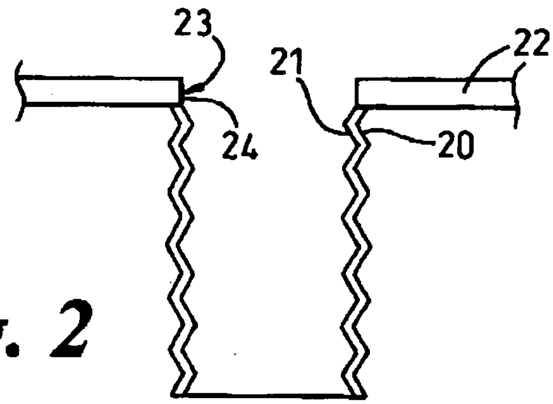


Fig. 2

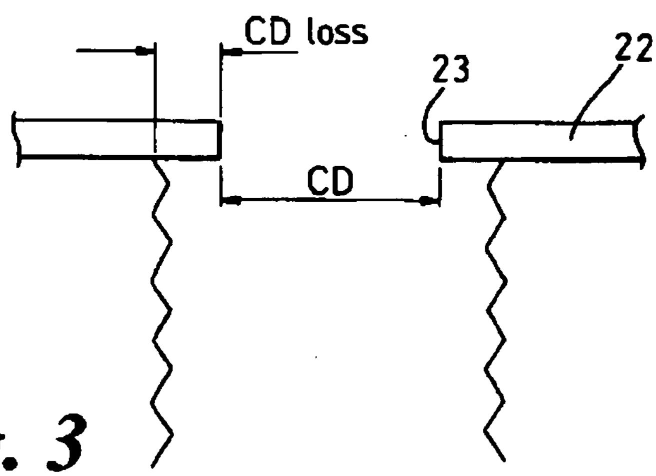


Fig. 3

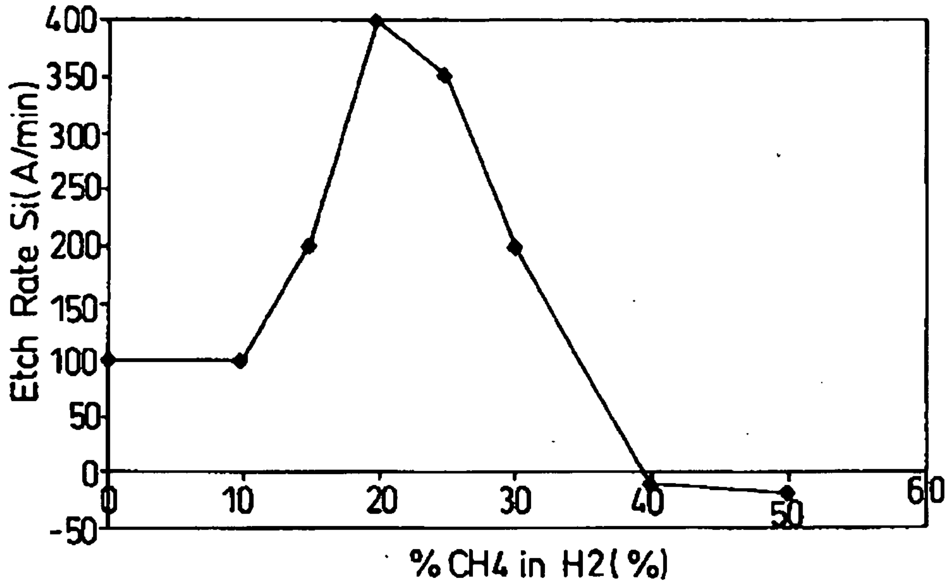

Etch Rate Si(A/min)
400
350
300
250
200
150
100
50
0
-50
0
10
20
30
40
50
60
% CH4 in H2(%)

Fig. 4

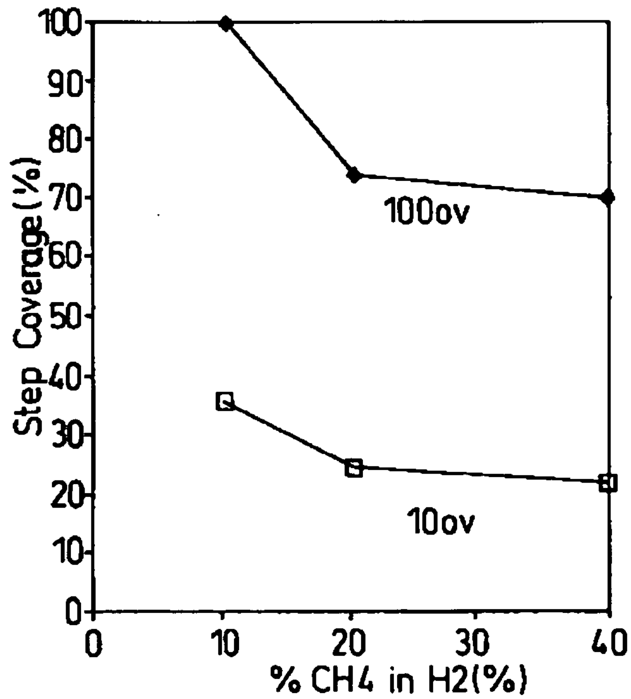

Step Coverage(%)
100
90
80
70
60
50
40
30
20
10
0
100ov
10ov
0
10
20
30
40
% CH4 in H2(%)

Fig. 5

Fig. 6(a)

Fig. 6(b)

Fig. 6(c)

Fig. 6(d)

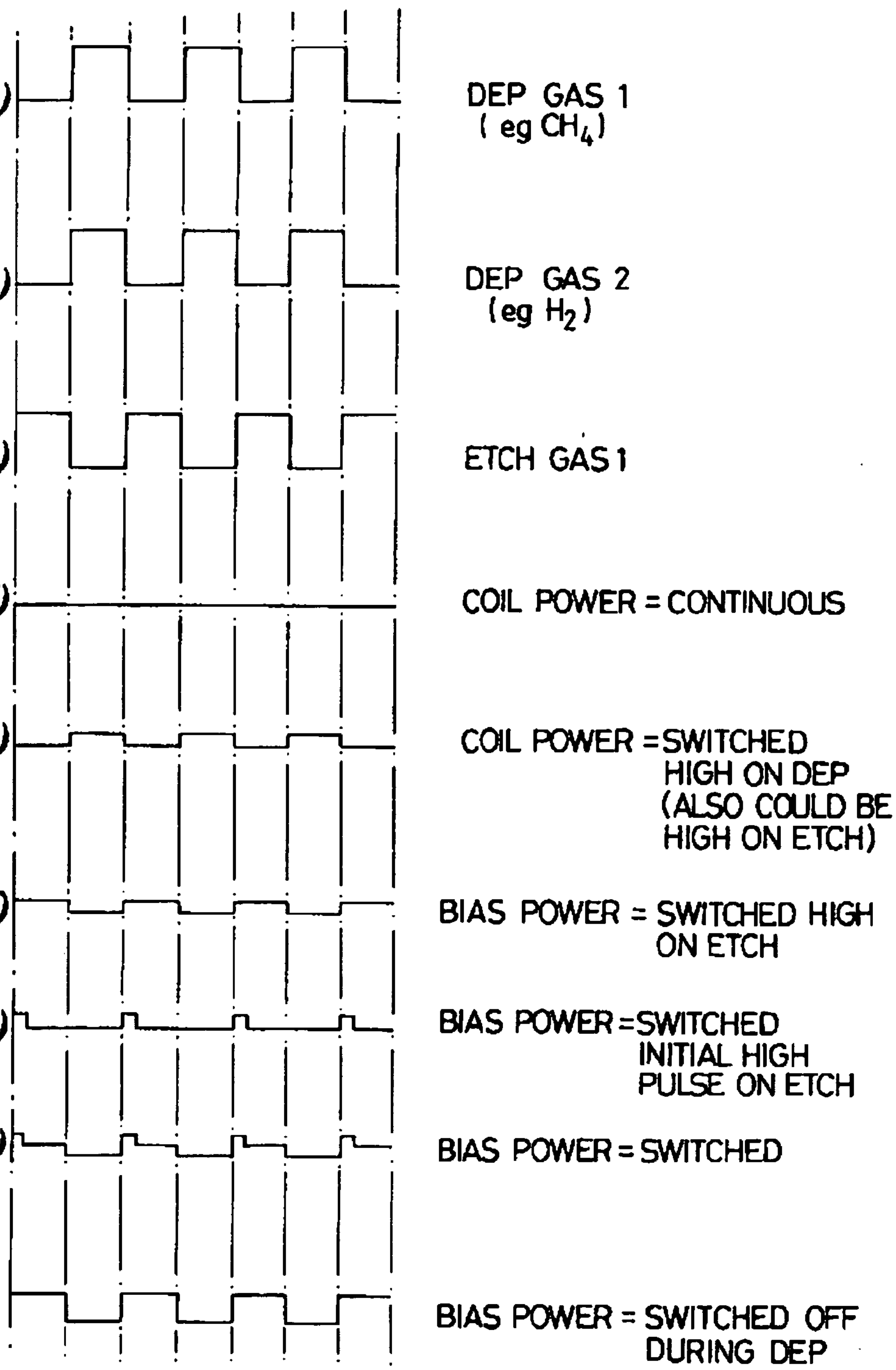
Fig. 6(e)

Fig. 6(f)

Fig. 6(g)

Fig. 6(h)

Fig. 6(i)



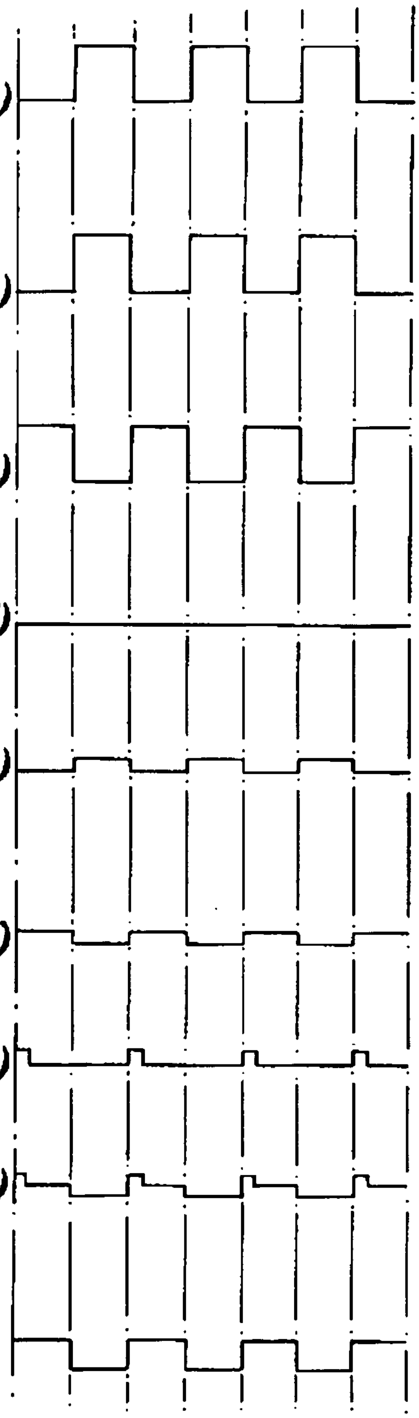


Fig. 6(a) DEP GAS 1 (eg CH_4)

Fig. 6(b) DEP GAS 2 (eg H_2)

Fig. 6(c) ETCH GAS 1

Fig. 6(d) COIL POWER = CONTINUOUS

Fig. 6(e) COIL POWER = SWITCHED HIGH ON DEP (ALSO COULD BE HIGH ON ETCH)

Fig. 6(f) BIAS POWER = SWITCHED HIGH ON ETCH

Fig. 6(g) BIAS POWER = SWITCHED INITIAL HIGH PULSE ON ETCH

Fig. 6(h) BIAS POWER = SWITCHED

Fig. 6(i) BIAS POWER = SWITCHED OFF DURING DEP

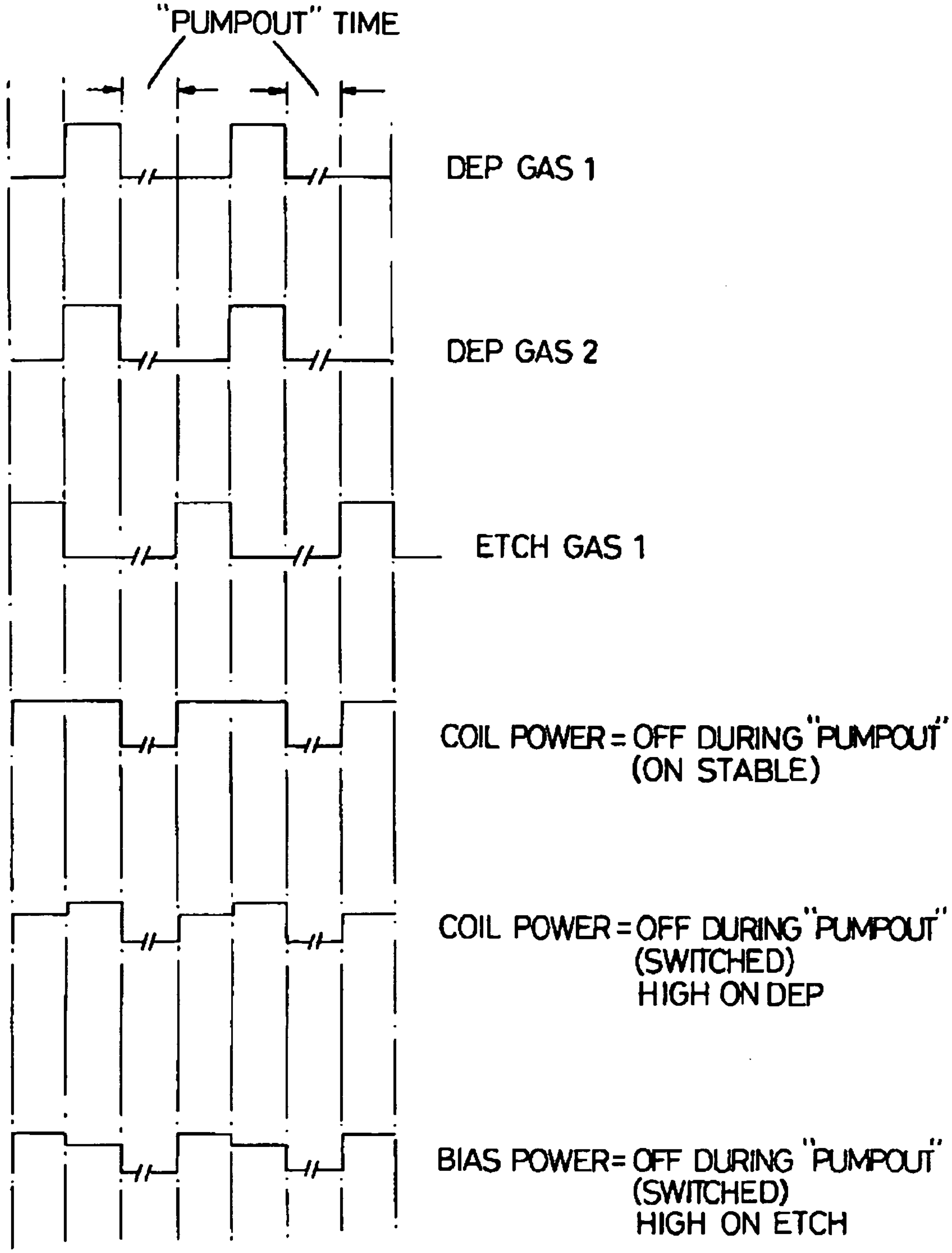
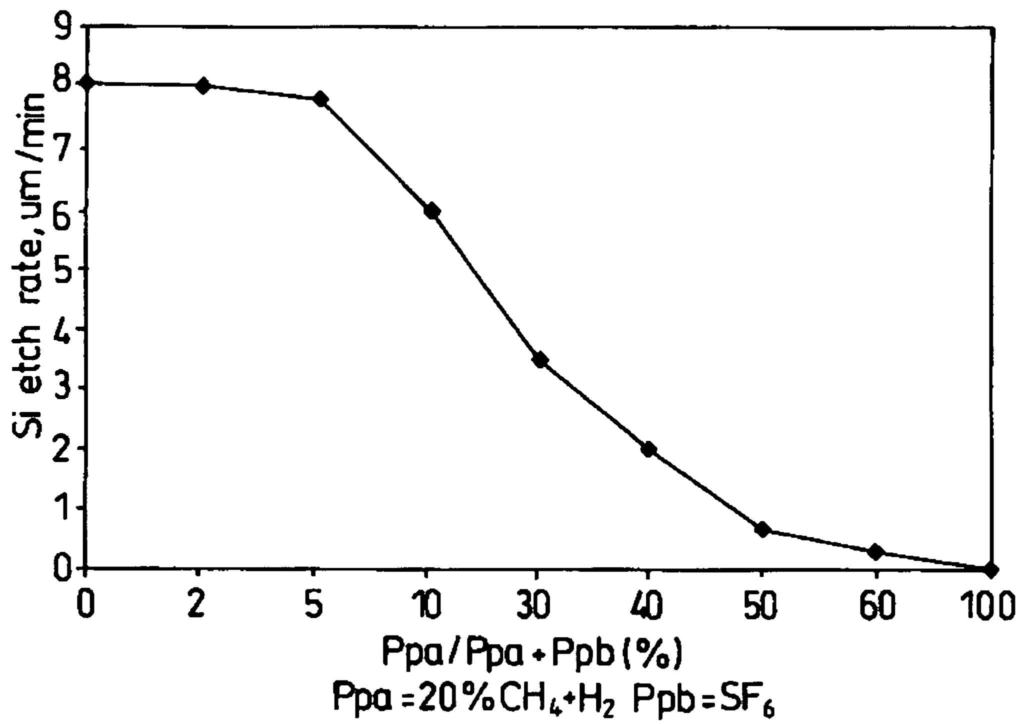

"PUMPOUT" TIME
DEP GAS 1
DEP GAS 2
ETCH GAS 1
COIL POWER = OFF DURING "PUMPOUT" (ON STABLE)
COIL POWER = OFF DURING "PUMPOUT" (SWITCHED) HIGH ON DEP
BIAS POWER = OFF DURING "PUMPOUT" (SWITCHED) HIGH ON ETCH

Fig. 7



Si etch rate, um/min
0
1
2
3
4
5
6
7
8
9
0
2
5
10
30
40
50
60
100
Ppa/Ppa+Ppb (%)
Ppa=20% CH_4+H_2 Ppb=SF_6

Fig. 8

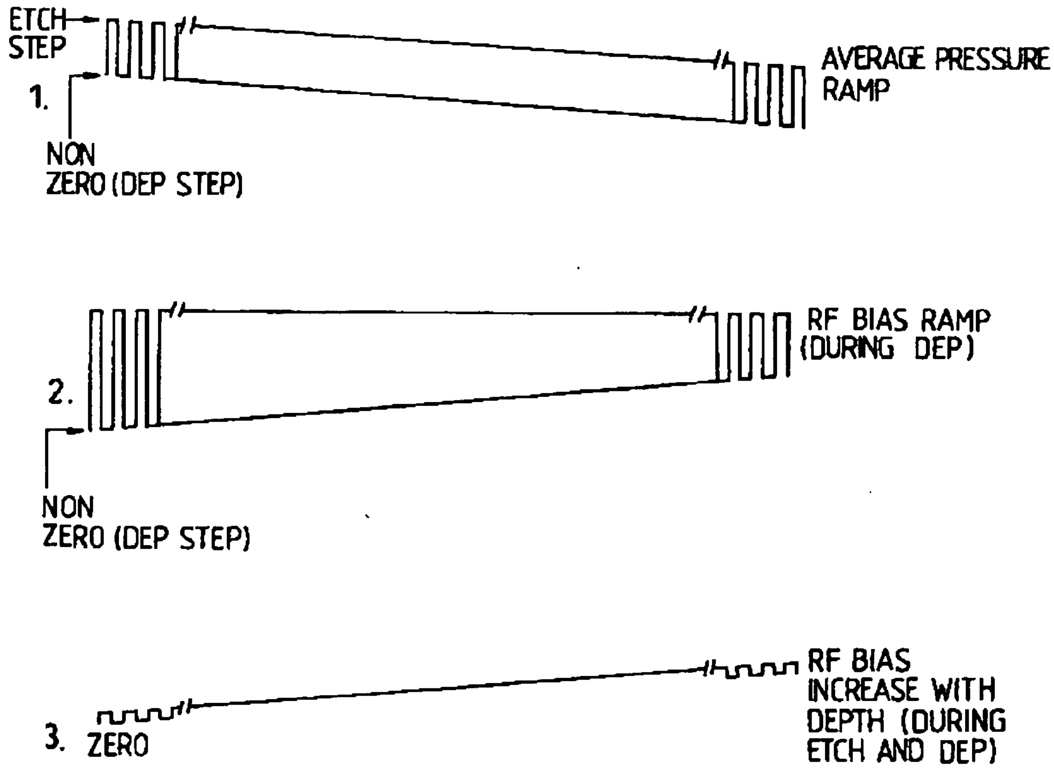


Fig. 9(i)

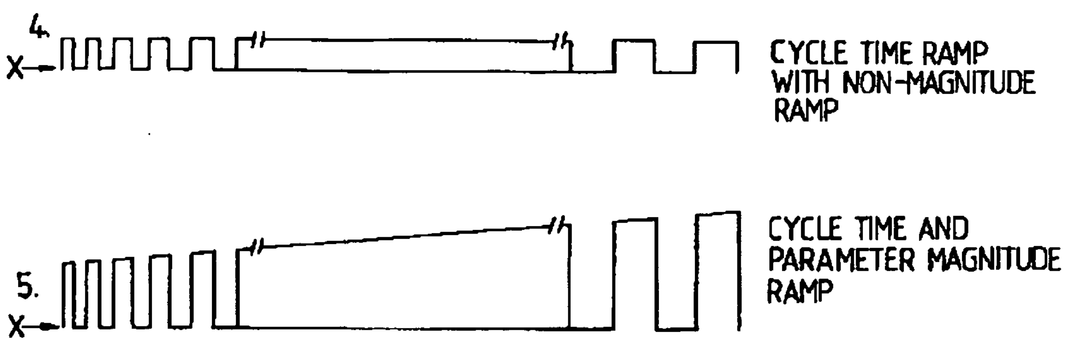


Fig. 9(ii)

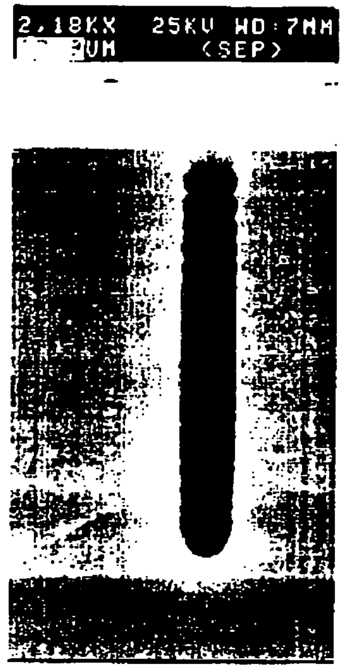


Fig. 10

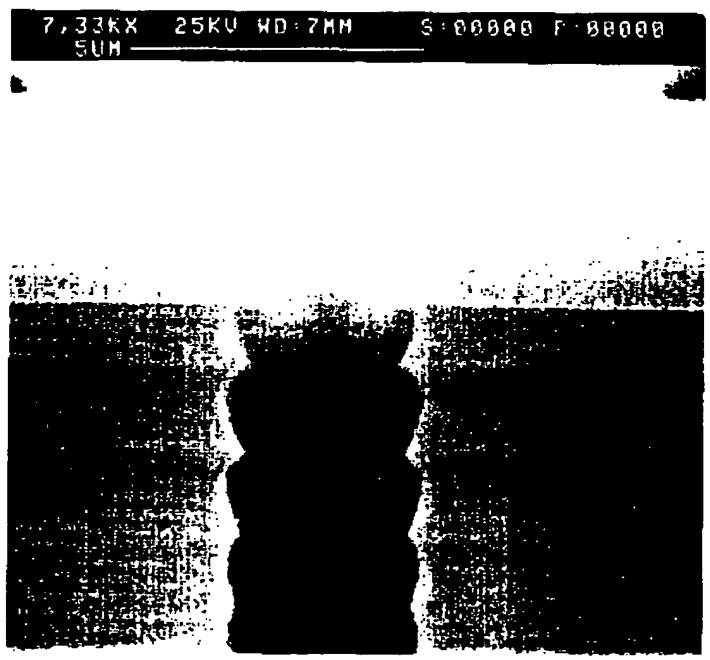


Fig. 11

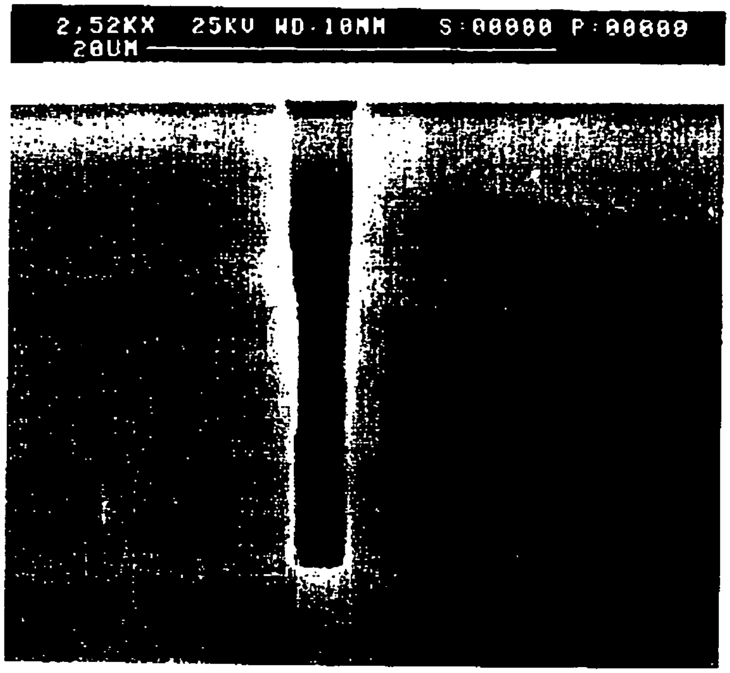

2,52KX 25KV WD·10MM S:00000 P:00000
20UM

Fig. 12

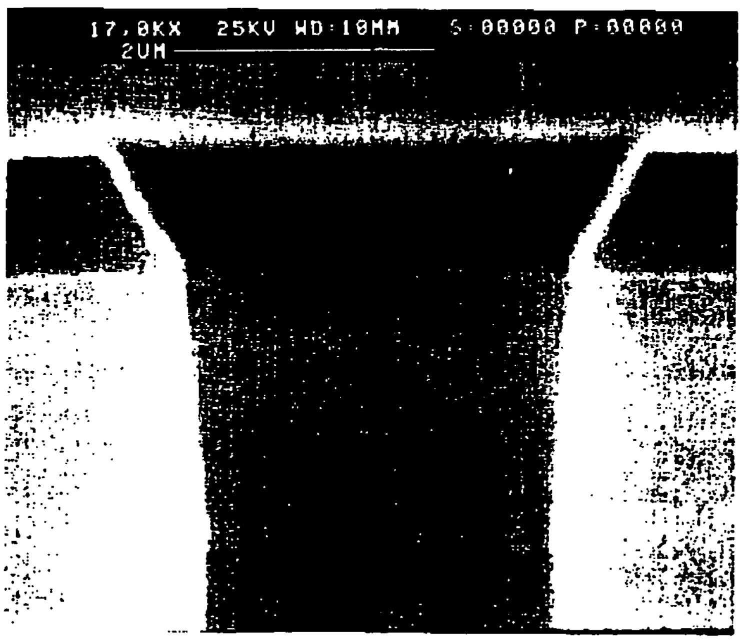

17,0KX 25KV WD:10MM S:00000 P:00000
2UM

Fig. 13

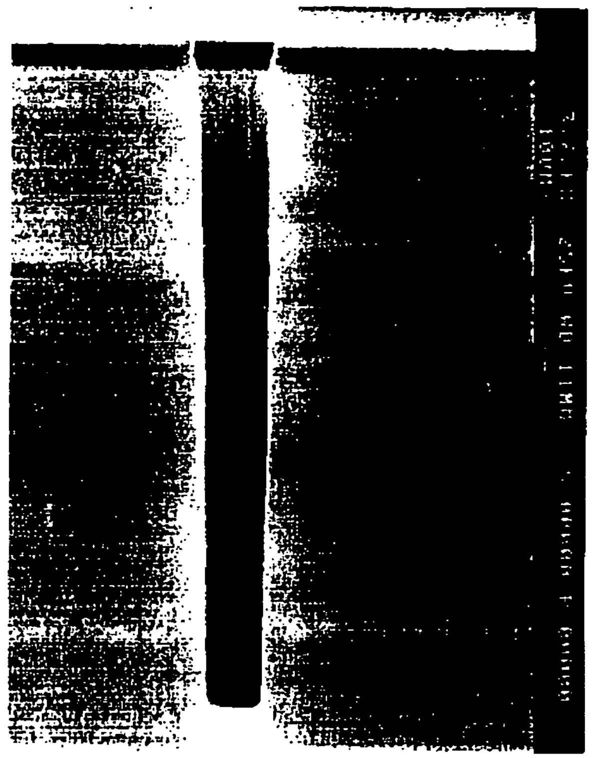


Fig. 14

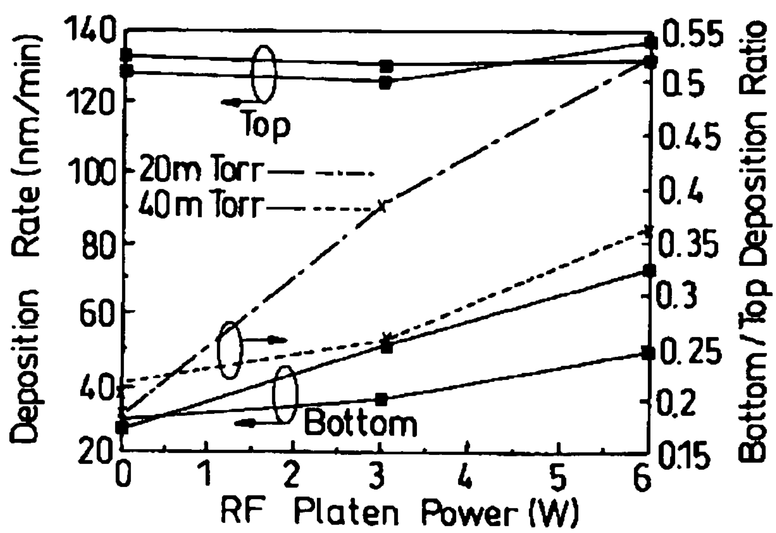

Deposition Rate (nm/min)
140
120
100
80
60
40
20
Bottom / Top Deposition Ratio
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0
1
2
3
4
5
6
RF Platen Power (W)
Top
Bottom
20m Torr
40m Torr

Fig. 15

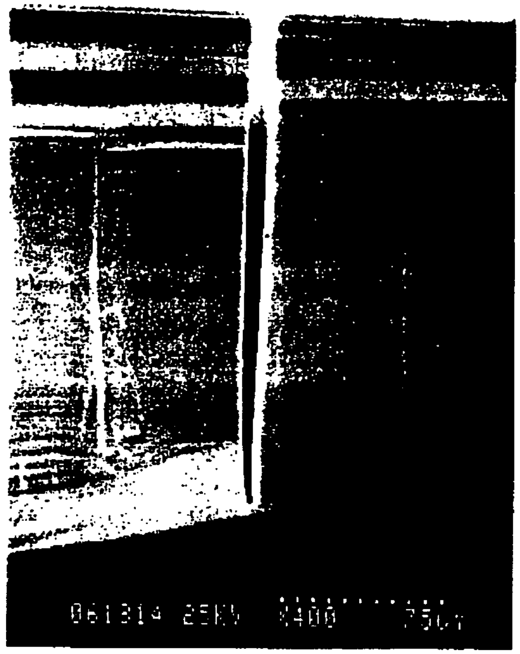


Fig. 16

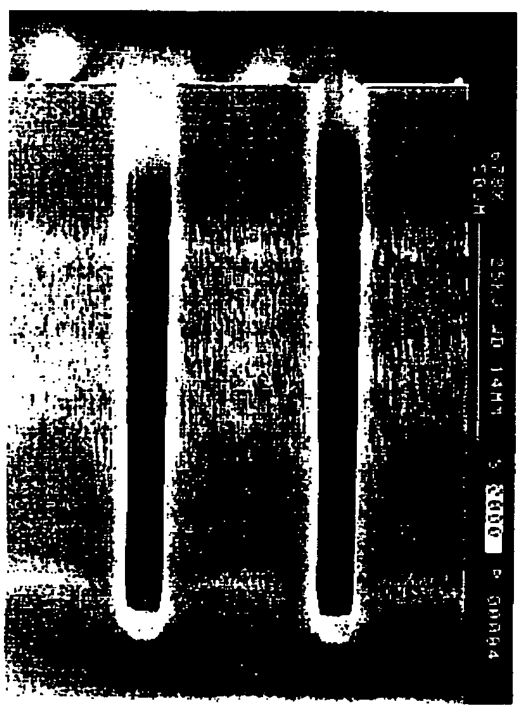


Fig. 17

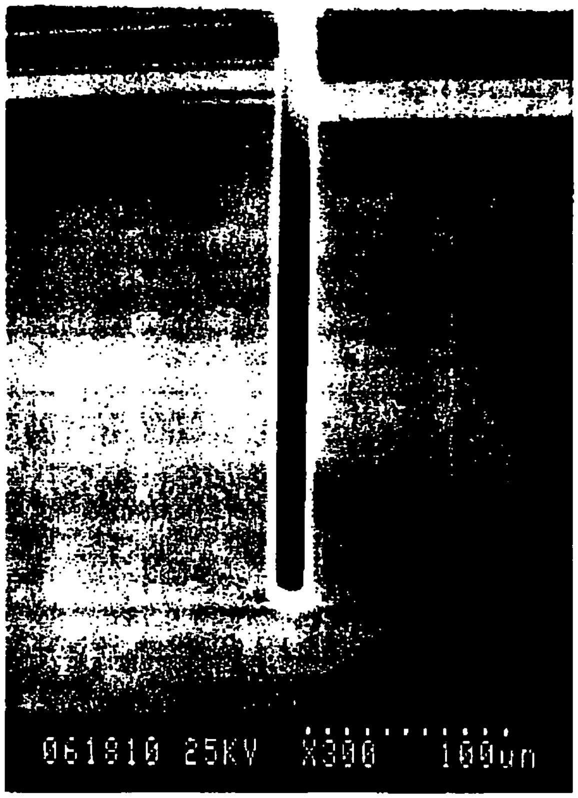


Fig. 18

Etch Step						Dep Step							Comments
Eflow (sccm) SF_6	Time (s)	Pressure (m Torr)	CoilP (W)	Platen P(W)		Pflow (sccm) C_4F_8		Time (s)	Pressure (m Torr)	CoilP (W)	Platen P(W)		(Figure 14) Ⓡ=Parameter Ramped
50 → 130 Ⓡ	13	25 → 35	600	12 → 10 Ⓡ		170 → 85 Ⓡ		7	38 → 21	600	0		Process Time = 8mins Etch Depth = 23 μm, Critical Dimension = 3μm Note Ramp only during first 10 cycles

Fig. 19(a)

Etch Step						Dep Step							Comments
Eflow (sccm) SF_6	Time (s)	Pressure (m Torr)	CoilP (W)	Platen P(W)		Pflow (sccm) C_4F_8		Time (s)	Pressure (m Torr)	CoilP (W)	Platen P(W)		(Figure 18) Ⓡ=Parameter Ramped
80	12	35 → 25 Ⓡ	600	10 → 12 Ⓡ		52		7	20 → 15 Ⓡ	600	0 → 5 Ⓡ		Process Time = 90 mins Etch Depth ~250μm, Critical Dimension up to 12 μm

Fig. 19(b)

Etch Step						Dep Step							Comments
Eflow (sccm) SF_6	Time (s)	Pressure (m Torr)	CoilP (W)	Platen P(W)		Pflow (sccm) C_4F_8		Time (s)	Pressure (m Torr)	CoilP (W)	Platen P(W)		(Figure 14) Ⓡ = Parameter Ramped
50 → 130	13	25 → 35	600	12 → 10		170 → 85		7	38 → 21	600	0		Process Time = 8 mins Etch Depth = 23 µm, Critical Dimension = 3µm Note Ramp only during first 10 cycles
Ⓡ				Ⓡ		Ⓡ							

Fig. 19(a)

Etch Step						Dep Step							Comments
Eflow (sccm) SF_6	Time (s)	Pressure (m Torr)	CoilP (W)	Platen P(W)		Pflow (sccm) C_4F_8		Time (s)	Pressure (m Torr)	CoilP (W)	Platen P(W)		(Figure 18) Ⓡ = Parameter Ramped
80	12	35 → 25	600	10 → 12		52		7	20 → 15	600	0 → 5		Process Time = 90 mins Etch Depth ~250µm, Critical Dimension up to 12 µm
		Ⓡ		Ⓡ					Ⓡ		Ⓡ		

Fig. 19(b)

Etch Step						Dep Step							Comments
Eflow (sccm) SF_6	Time (s)	Pressure (m Torr)	Coil P (W)	Platen P (W)		Pflow (sccm) C_4F_8		Time (s)	Pressure (m Torr)	Coil P (W)	Platen P (W)		(Figure 14) (R) = Parameter Ramped
50 → 130	13	25 → 35	600	12 → 10		170 → 85		7	38 → 21	600	0		Process Time = 8mins Etch Depth = 23 μm, Critical Dimension = 3μm Note Ramp only during first 10 cycles
(R)				(R)		(R)							

Fig. 19(a)

Etch Step						Dep Step							Comments
Eflow (sccm) SF_6	Time (s)	Pressure (m Torr)	Coil P (W)	Platen P (W)		Pflow (sccm) C_4F_8		Time (s)	Pressure (m Torr)	Coil P (W)	Platen P (W)		(Figure 18) (R) = Parameter Ramped
80	12	35 → 25	600	10 → 12		52		7	20 → 15	600	0 → 5		Process Time = 90 mins Etch Depth ~250μm, Critical Dimension up to 12 μm
		(R)		(R)					(R)		(R)		

Fig. 19(b)

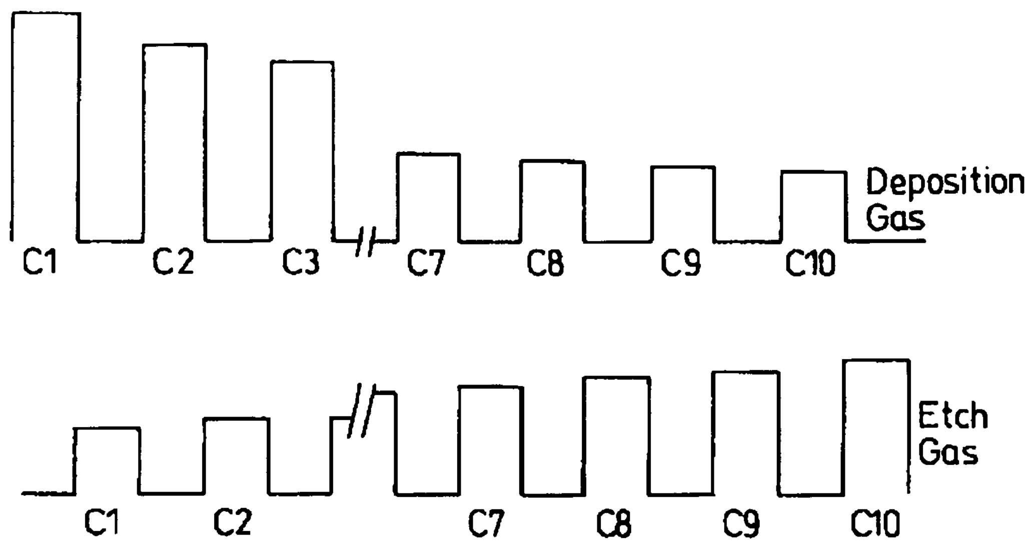

Deposition
Gas
C1
C2
C3
C7
C8
C9
C10
Etch
Gas
C1
C2
C7
C8
C9
C10

Fig. 20

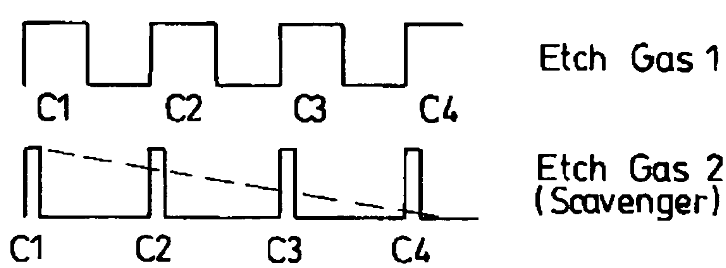

Etch Gas 1
C1
C2
C3
C4
Etch Gas 2
(Scavenger)
C1
C2
C3
C4

Fig. 21